REMARKS

Claims 1 and 7 are canceled. Claims 13 and 14 are added. Therefore, claims 2-6 and 8-13 are the claims pending in the Application.

Applicant acknowledges that the rejection of claims 1-12 under 35 U.S.C. § 101 has been withdrawn.

Applicant thanks the Examiner for reviewing and considering the references cited in the Information Disclosure Statement filed on October 11, 2000.

Applicant thanks the Examiner for approving the proposed drawing correction for Fig. 1. The previous Amendment filed August 27, 2002 erroneously states that a proposed drawing correction to Fig. 3 was being submitted. Fig. 3 needs no correction except as required by the Draftsperson. Responsive to the objection of the Draftsperson, corrected Formal Drawings of Figs. 1- 6 are submitted herewith.

Claim Rejections - 35 U.S.C. § 112, First Paragraph

Claims 3 and 5 are rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. This rejection is traversed.

The Examiner alleges that the phrase "based on a value V_C of a transistor property of a transistor included in the logic block" of amended claim 3 is new subject-matter.

Page 9-14 of the written disclosure as originally filed provides ample support for claims 3 and 5. By way of illustrative example, and not by way of limitation of the scope of the claims,

expression (2) on page 10 provides that C_{in}, the load capacitance of a transistor connected to the input pin, is used to calculate S_{in}, the stress of an input pin. S_{in} is then used to calculate the time degradation rate of an input pin according to expression (1) on page 9. The time degradation rate of an input pin is used to calculate the pin-to-pin delay time, as described in detail, for example, on pages 10-11. Therefore, a value V_C of a transistor property of a transistor included in the logic block is used to calculate pin-to-pin delay time. Applicant's claimed invention encompasses several embodiments and the foregoing discussion is meant to provide only an illustrative example, not to restrict the scope of the embodiments disclosed or to limit the scope of the claims. Therefore, it is respectfully submitted that a person of ordinary skill in the art would have understood that Applicant had possession of the claimed invention at the time the application was filed. Accordingly, the Examiner is requested to withdraw the rejection of claim 3.

The Examiner rejected claim 5 because of its dependency from claim 3. Since claim 3 is believed to be in patentable form, the Examiner is requested to withdraw the rejection of claim 5.

Claim Rejections - 35 U.S.C. § 112

Claims 3-6 and 9-12 are rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. This rejection is traversed.

With respect to Examiner's first point, the Examiner cites lines 2-4 of Page 4 and lines 15-17 of page 6 of the Specification and states that it is unclear how "two logic blocks" are "connected to each other by a computer" (Office Action, Page 4, emphasis added). The two cited sentences of the Specification contains the preposition "by" instead of "in." The Specification is amended. It is respectfully submitted that a person of ordinary skill in the art would have understood at the time the Application was filed that logic blocks of a logic-level circuit may be arranged on an integrated circuit or chip and are typically arranged in a computer. The Examiner is requested to withdraw the rejection on this basis.

With respect to the Examiner's second point on Page 5 of the Office Action about three stage inverter expressions (31) and (32) on page 19 and expression (33) and (34) on page 20 of the Specification, Applicant notes that as known in the art, if an input to an inverter changes from a low level to a high level, then the hot carrier effect may cause damage to the inverter. On the contrary, if the input to the inverter changes from high to low, then no damage to the inverter is caused by the hot carrier effect.

Under these circumstances, if a logic block including inverters, which are consecutively numbered 1, 2, ...N, receives an input which changes from a low level to a high level, then the odd-numbered inverters 1, 3, 5, ... 2n+1 receive hot carrier damage, while the even-numbered inverters 2, 4, 6, ... 2n receive no hot carrier damage (N, n: natural number), and vice versa if the input changes from the high level to the low level.

More specifically, the expression (31) shows values of λ_{in} and λ_{out}, in the case where the logic block includes three inverters and an input to the logic block changes from a low level to a high level. The inverter at the input stage of the first (odd-numbered) inverter receives hot

carrier damage. Consequently, $\lambda_{in} = 1/3$. The inverter at the output stage or the third (odd-numbered) inverter receives hot carrier damage. Consequently, $\lambda_{out} = 1/3$.

On the other hand, the expression (32) shows values of λ_{in} and λ_{out}, in the case where an input to the logic block changes from the high level to the low level. In this case, the input and the output stage inverters are subjected to no damage. Consequently, $\lambda_{in} = 0$ and $\lambda_{out} = 0$.

The expression (33) shows values of λ_{in} and λ_{out}, in the case where the logic block includes four inverters and an input to the logic block changes from a low level to a high level. The inverter at the input stage, or the first (odd-numbered) inverter receives hot carrier damage. Consequently, $\lambda_{in} = 1/4$. The inverter at the output stage, or the fourth (even-numbered) inverter receives no hot carrier damage. Consequently, $\lambda_{out} = 0$.

The expression (34) shows values λ_{in} and λ_{out}, in the case where the logic block includes four inverters and an input to the logic block changes from a high level to a low level. The input stage inverter receives no hot carrier damage. Consequently, $\lambda_{in} = 0$. The output stage inverter receives hot carrier damage. Consequently, $\lambda_{out} = 1/4$.

Claim Rejections - 35 U.S.C. § 112

Claims 7-12 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter, which applicant regards as the invention. This rejection is traversed.

The Examiner is correct that "the product" on line 4 of claim 7 refers to the "program" mentioned earlier in the claim. Similarly in claims 9-11, "the product" refers to the "program"

mentioned earlier in each of those claims. It is respectfully submitted that a person of ordinary skill in the art would have understood the claims as filed, just as the Examiner was able correctly to understand them. Nevertheless, claims 7 and 9-11 are amended to use the language suggested by the Examiner. These are not a narrowing amendment. No estoppel is created.

Claim 8 was rejected because of its dependence from claim 7. Since claims 7-11 are now believed to be in patentable form, the Examiner is requested to withdraw the rejection.

Claim Rejections - 35 U.S.C. § 102

Claims 9 and 11 are rejected under 35 U.S.C. § 102(e) as being anticipated by Iwanishi, et al., U.S. Patent No. 6,047,247. This rejection is traversed.

Claims 9 requires calculating variations of signal delay times caused by aging, based only on values for the transistors connected directly to the input and output pins of logic blocks. Claim 11 incorporates this calculation by reference to claim 9.

Iwanishi discloses a method of estimating hot carrier-delay degradation based on circuit information 11 and a delay library 12. The circuit information includes characteristic information of the cells, information of connection between cells and the cell-to-cell wirings such as resistance values and capacitance values. Iwanishi, col. 2, lines 59-63. The delay library contains delay parameters, such as coefficients and points of the tables used for cell delay tables, where the cell delay tables are functions with respect to input signal waveform inclinations (slew) and output load capacitance. Iwanishi, col. 7, lines 59-65. Iwanishi does not disclose or suggest calculating signal delay times caused by aging, based on a transistor property of a

transistor included in the logic block. Further, Iwanishi does not disclose or suggest calculating signal delay times caused by aging based on values for the transistors connected directly to the input and output pins of logic blocks. Therefore, Iwanishi does not disclose or suggest all the recitations of claims 9 and 11.

Claim Rejections - 35 U.S.C. § 103

Claims 1-2 and 7-8 are rejected under 35 U.S.C. § 103(a), as obvious over Iwanishi, et al. in view of Fang, et al., U.S. Patent No. 6,278,964. This rejection is traversed.

Claims 1 and 7 are canceled, and therefore the rejection is moot as to these claims.

Claim 2 requires calculating V_B, a block property of a logic block included in the logic level circuit, from a plurality of numerical values V_C, wherein the plurality of V_C values includes exclusively a first group of V_C values of transistors connected directly to an input pin of the logic block and a second group of V_C values of transistors connected directly to an output pin of the logic block. Further, claim 8 requires calculating V_B, a block property of a logic block included in the logic level circuit, from a plurality of numerical values V_C, wherein the plurality of V_C values includes a V_C value of a transistor connected directly to an input pin of the logic block and another V_C value of a transistor connected directly to an output pin of the logic block.

The Examiner acknowledges that Iwanishi does not disclose that each V_C value represents a transistor property of transistor included in the logic block.

Fang discloses a hot-carrier effect simulation for integrated circuits, in which various types of data, including information about transistors. (E.g. Fang, col. 6, lines 53-64.) Fang does

not disclose or suggest calculating V_B, a block property of a logic block included in the logic level circuit, based on transistor values for transistors directly connected to the input pins and the output pins in a logic block. Further, Fang does not disclose or suggest this calculation based on transistor values for transistors directly connected to the input pins and the output pins in a logic block.

Further, there is no motivation for combining Iwanishi and Fang to arrive at Applicant's claimed invention. One of the problems recognized and solved by Applicant's claimed invention is the need to calculate the hot-carrier effect faster and more simply by using fewer variables. Iwanishi and Fang do not identify this problem, let alone disclose the solutions provided by Applicant's claimed invention. Therefore, it is respectfully submitted that a person of ordinary skill in the art would not have been led to Applicant's claimed invention based on Iwanishi and Fang.

New claims 13 and 14 are added. These claims contain no new matter. (See by way of example, not by way of limitation, pages 8-14 of the Specification.) These claims are patentably distinguishable over the prior art for at least reasons analogous to those applicable to claims 2-6 and 8-12 as set forth above.

A Petition for Extension of Time for a one (1) month extension is attached herewith. A Submission of Drawings with Figures 1-6 is attached herewith.

In view of the foregoing remarks, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the

Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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PATENT TRADEMARK OFFICE

Date: April 1, 2003

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The specification is changed as follows:

Paragraph bridging pages 3 and 4:

According to this invention, a method for calculating pin-to-pin delay time T_{iopath_aged} and block-to-block delay time $T_{connect\_aged}$ is provided. The pin-to-pin delay time T_{iopath_aged} is delay time of a signal passing between an input pin and an output pin of a logic block. The block-to-block delay time $T_{connect\_aged}$ is delay time of a signal passing between said two logic blocks connected to each other ~~by~~ in a computer. Furthermore, this method comprises the following steps:

Page 6, first full paragraph:

According to this invention, a computer software product for calculating pin-to-pin delay time T_{iopath_aged} and block-to-block delay time T_{iopath_aged} is provided. The pin-to-pin delay time T_{iopath_aged}, is delay time of a signal passing between an input pin and an output pin of a logic block. The block-to-block delay time $T_{connect\_aged}$, which is delay time of a signal passing between said two logic blocks connected to each other ~~by~~ in a computer. And then, the computer software product makes a computer execute the following processes:

IN THE CLAIMS:

Claims 1 and 7 are canceled.

The claims are amended as follows:

2. (Twice Amended) A method of calculating, by the use of a computer, a numerical value V_A representative of a circuit property of a logic level circuit, from a numerical value V_B, which shows a block property of a logic block included in the logic level circuit, the method comprising:

(a) calculating the value V_B from a plurality of numerical values V_C, each value V_C representing a transistor property of a transistor included in the logic block; and,

(b) calculating the value V_A from the value V_B, and outputting the value V_A as a value representative of a circuit property of said logic level circuit

~~A method as in claim 1,~~ wherein, in the step (a), the plurality of values V_C comprises ~~each of~~ a first group of V_C values ~~of said plurality of numerical values V_C shows a specific transistor property of~~ a transistors connected directly to an input pin of the logic block and ~~each of~~ a second group of V_C values ~~of said plurality of numerical values V_C shows another specific transistor property of~~ a transistors connected directly to an output pin of the logic block.

3. (Twice Amended) A method of calculating, by the use of a computer, a delay time of a signal passing through a logic level circuit which consists of a plurality of logic blocks from pin-to-pin delay time, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time, which is delay time of a signal passing between two logic blocks connected to each other, comprising:

(a) calculating the pin-to-pin delay time, based on a value V_C of a transistor property of a transistor included in the logic block, and the block-to-block delay time without calculating in aging caused by hot carrier effect;

(b) calculating variations of signal delay times caused by aging, based on ~~that signals pass through~~ the value V_C of a transistors~~s~~ connected to the input pin and the value V_C of a transistor connected to the output pin ~~caused by said aging~~; and,

(c) modifying the pin-to-pin delay time and the block-to-block delay time calculated in step (a) by the variations calculated in step (b), and outputting said modified values for use as values representative of circuit properties of said logic level circuit.

4. (Twice Amended) A method of calculating, by the use of a computer, pin-to-pin delay time T_{iopath_aged}, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time $T_{connect\_aged}$, which is delay time of a signal passing between said two logic blocks connected to each other, comprising:

(a) calculating an amount of stress S_{in} cast by the input pin and an amount of stress S_{out} cast by the output pin according to the following expression:

~~when it is assumed that a load capacitance is represented by C [pF], constants~~

$$S = \alpha\left(\frac{C}{W}\right)^{\beta}$$

where a load capacitance is represented by C [pF], constants depending on change of inputted waveform are represented by α and β, and width of channel of the transistor connected to the pin is represented by W [μm];

(b) calculating an aged delay time of the input pin δ_{in} [%] and an aged delay time δ_{out} [%] according to the following expression:

~~when it is assumed that a constant depending on physical structure of the pin~~

$$\delta = \gamma \left(\frac{\tau S f}{\varepsilon_1 e^{\kappa T}} \right)^{\frac{1}{\varepsilon_2}}$$

where a constant depending on physical structure of the pin is represented by γ, the term of guarantee of the LSI is represented by τ [hour], constants depending on process are represented by $\varepsilon 1$, $\varepsilon 2$ and κ, working frequency is represented by f [Hz], and absolute temperature is represented by T [K];

(c) calculating and outputting for use as values representative of circuit properties of said logic level circuit the pin-to-pin delay time T_{iopath_aged} and the block-to-block delay time $T_{connect\_aged}$ according to the following expressions:

~~when it is assumed that pin-to-pin delay time and block-to-block delay time~~

$$T_{iopath\_aged} = T_{iopath\_fresh}\left(1 + \lambda_{in}\delta_{in} + \lambda_{out}\delta_{out}\right)$$
$$T_{connect\_aged} = T_{connect\_fresh}\left(1 + \lambda_{out}\delta_{out}\right)$$

where pin-to-pin delay time and block-to-block delay time calculated ignoring aging caused by hot carrier effect are represented by T_{iopath_fresh} [ps] and $T_{connected\_fresh}$ [ps], and ratios of delay

times occurred at the input stage and the output stage to whole delay time occurred from the input pin to the output pin are represented by λin and λout.

8. (Twice Amended) A computer-readable medium incorporating a program of instructions for calculating a numerical value V_A which shows a property of a logic level circuit, from a numerical value V_B, which shows a property of a logic block constituting the logic level circuit, the program making a computer execute the following processes:

(a) calculating the V_B value from a plurality of numerical values V_C, each V_C value showing a property of a transistor constituting part of the logic block; and,

(b) calculating the V_A value from the V_B value, and outputting the V_A value for use as a value representative of a circuit property of said logic level circuit,

~~A computer readable medium incorporating a program of instructions as in claim 7~~ wherein in process (a) the plurality of ~~one~~ V_C values comprises a V_C value ~~shows a property~~ of a transistor connected directly to an input pin of the logic block and another V_C value ~~shows a property of~~ a transistor connected directly to an output pin of the logic block.

9. (Twice Amended) A computer-readable medium incorporating a program of instructions for calculating a delay time of a signal passing through a logic level circuit which includes ~~consists of~~ a plurality of logic blocks from pin-to-pin delay time, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time, which is delay time of a signal passing between two logic blocks connected to each other, the program ~~product~~ making a computer execute the following processes:

(a) calculating the pin-to-pin delay time and the block-to-block delay time without calculating in aging caused by hot carrier effect;

(b) calculating variations of signal delay times caused by aging, based on ~~that signals pass through~~ values for the transistors connected directly to the input and output pins~~-~~ of logic blocks ~~caused by said aging~~; and,

(c) modifying the pin-to-pin delay time and the block-to-block delay time calculated in step (a) by the variations calculated in step (b), and outputting said modified values for use as values representative of circuit properties of said logic level circuit.

10. (Twice Amended) A computer-readable medium incorporating a program of instructions for calculating pin-to-pin delay time T_{iopath_aged}, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time $T_{connect\_aged}$, which is delay time of a signal passing between said two logic blocks connected to each other by a computer, the program ~~product~~ making a computer execute the following processes:

(a) calculating an amount of stress S_{in} cast by the input pin and an amount of stress S_{out} cast by the output pin according to the following expression:

~~when it is assumed that a load capacitance is represented by C [pF], constants~~

$$S = \alpha\left(\frac{C}{W}\right)^{\beta}$$

where a load capacitance is represented by C [pF], constants depending on change of inputted waveform are represented by α and β, and width of channel of the transistor connected to the pin is represented by W [μm];

(b) calculating an aged delay time of the input pin δ_{in} [%] and an aged delay time δ_{out} [%] according to the following expression:

~~when it is assumed that a constant depending on physical structure of the pin~~

$$\delta = \gamma\left(\frac{\tau S f}{\varepsilon_1 e^{\kappa T}}\right)^{\frac{1}{\varepsilon_2}}$$

where that a constant depending on physical structure of the pin is represented by γ, the term of a guarantee of the LSI is represented by τ [hour], constants depending on process are represented by $\varepsilon 1$, $\varepsilon 2$ and κ, working frequency is represented by f [Hz], and absolute temperature is represented by T [K];

(c) calculating and outputting for use as values representative of circuit properties of said logic level circuit the pin-to-pin delay time T_{iopath_aged} and the block-to-block delay time $T_{connect\_aged}$ according to the following expressions:

$$T_{iopath\_aged} = T_{iopath\_fresh}\left(1 + \lambda_{in}\delta_{in} + \lambda_{out}\delta_{out}\right)$$
$$T_{connect\_aged} = T_{connect\_fresh}\left(1 + \lambda_{out}\delta_{out}\right)$$

where ~~n it is assumed that~~ pin-to-pin delay time and block-to-block delay time calculated ignoring aging caused by hot carrier effect are represented by T_{iopath_fresh} [ps] and $T_{connected\_fresh}$ [ps], and ratios of delay times occurred at the input stage and the output stage to whole delay time occurred from the input pin to the output pin are represented by λ_{in} and λ_{out}, respectively.

11. (Twice Amended) A computer-readable medium incorporating a program of instructions for calculating a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, the program ~~product~~ making a computer execute the following processes:

(a) calculating delay times of all said logic blocks according to the program ~~product~~ as in claim 9; and,

(b) calculating and outputting for use as a value representative of a circuit property of said logic level circuit the delay time of the logic level circuit from the result of step (a).

12. (Twice Amended) A computer-readable medium incorporating a program of instructions for calculating a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, the program ~~product~~ making a computer execute the following processes:

(a) calculating delay times of all said logic blocks according to the program ~~product~~ as in claim 10; and,

(b) calculating and outputting for use as a value representative of a circuit property of said logic level circuit the delay time of the logic level circuit from the result of step (a).

Claims 13 and 14 are added as new claims.